A small-area low-power low-noise instrumentation amplifier (IA) is desired in arrayed sensor devices that are used for high-spatial-resolution biomedical and environment monitoring systems. This paper presents a 0.06mm² chopper-stabilized current-feedback IA with 13.5nV/√Hz input-referred noise and less than 3.5μV offset voltage. For significantly reducing the ripple due to choppings, the proposed IA uses a novel digital calibration scheme, namely, automatic differential-pair matching (ADPM), which enables a small die area and low-power operation. The proposed IA is implemented in a standard 0.18μm CMOS and achieves a noise efficiency factor (NEF) of 7.2 while drawing 194μA. The active area of the IA is 7.6x smaller than that of the state-of-the-art [1-5] while it maintains low output ripple, low noise, and low power.

Many chopper-stabilized IAs suffer from a ripple voltage which is the result of modulation of the amplifier’s offset voltage. Such IAs usually utilize several filtering techniques to reduce the unintended output ripple, e.g., ripple reduction loop [1, 3] and switched-capacitor notch filter [2, 4, 5]. These conventional ripple-reduction techniques are based on analog schemes, and consume static power and a large die area for the passive components. Since the proposed ripple-reduction technique uses a digital calibration approach, power and area can be drastically saved as compared to the corresponding analog schemes.

Figure 10.4.1 shows the block diagram of the complete IA system. The chip includes a main amplifier, a current-feedback path to configure IA with a stable gain, a detector, and a calibration logic for ADPM. The main amplifier path is based on a three-stage opamp topology. It uses the single-capacitor active feedback compensation (SCAFC) technique [6], which also enables small-area realization compared to a nested Miller compensation. A differential pair in the first stage of the amplifier is composed of common-source 12-separated (or fingered) MOSFETs. These 12 MOSFETs, despite the careful layout, have mismatches that follow a normal probability distribution, thereby the differential pair also has a systematic offset voltage. In this design, the 12 MOSFETs for the differential pair are reconfigurable and can be used in either the positive input side or the negative one as controlled by a digital code S. Therefore, if the best combination for minimizing the input-referred offset of the differential pair is found, the ripple voltage can be significantly reduced. Since there are 12 MOSFETs, the number of possible combination patterns is calculated as \(2^{12} = 924\). The proposed calibration logic finds the best combination through the ADPM loop as shown in Fig.10.4.1. During the calibration (ENBL=H), the offset voltage due to the mismatch is measured at the detector through the non-chopping main amplifier with a closed-loop gain of 1000, which is determined by an on-chip resistor \(R_2\). The offset voltage is accurately detected because the main amplifier acts as a preamplifier with a high gain, thereby the following detector can sense the input-referred offset voltage of a few microvolts. The calibration logic receives the result of the detector and searches for the best combination pattern of the differential pair to minimize the offset voltage. The proposed digital calibration method for ADPM does not require any static power for reducing the ripple and furthermore, the detector and the calibration logic can be turned off when the calibration is finished. During the normal signal processing, the IA gain is set by an external resistor instead of the internal resistor \(R_2\).

Figure 10.4.2 shows the details of the calibration logic and the detector. The detector is a simple switched-capacitor latched comparator with an auto-zeroed preamplifier to reduce its offset voltage. The calibration logic has a lookup-table (LUT) for generating all combination patterns to reconfigure the differential pair, a register (MinReg) to store the pattern for the minimum offset combination, a clock generator, and a controller. An example timing diagram of a calibration operation is shown in Fig. 10.4.3. The calibration repeats four phases (a) to (d) for each combination pattern (LUT_out) generated from the LUT as shown in Fig. 10.4.3. The calibration is finished when all of the patterns are checked. The detailed operation for searching the best combination is as follows; first, sampling the output voltage \(V_{out}\) for a combination of LUT_out for which the equalizer (SEL) and checking the polarity of the output (b) are performed. If the polarity is positive, the data of SEL is held until the next phase (c). On the other hand, if the polarity is negative, a pull-up PDL_chng is activated and a code of SEL is inverted [see phase (e), for example]. In this case, 6 MOSFETs of the positive input side and the other 6 MOSFETs of the negative input side are simultaneously swapped with each other, and thus the sign of the IA’s output voltage is inverted as shown in Fig. 10.4.3(e). In phase (d), SEL is temporarily set to a value of MinReg which stores the best combination pattern at the time. Since switches \(S_{sw}\) keep turning on during this phase where the voltage \(V_{out}\) is stored on the capacitors \(C_{c}\), the voltage \(V_{out}\) is compared to \(V_{min,new}\) by using the comparator. Therefore, if \(V_{out}>V_{min,new}\), MinReg is not updated at this time. On the other hand, as shown in Fig.10.4.3(f), if \(V_{out}<V_{min,new}\), MinReg is updated as LUT_out1, which is a better combination pattern. The best combination pattern is then saved on the register MinReg and the systematic offset voltage is drastically suppressed, resulting in a low output ripple.

The prototype IA is fabricated in a 0.18μm CMOS technology with high-resistivity silicon-on-insulator (SOI) wafers, and the current dissipation is 194μA of which 2μA is for the digital part. Figure 10.4.7 shows a chip micrograph.

The effectiveness of the proposed calibration for ADPM can be confirmed by the histogram of the measured input-referred peak-to-peak ripple voltage as shown in Fig. 10.4.4. The average ripple voltage before calibration is 1.84mVpp, and it is reduced to 72μVpp by the proposed ADPM. Figure 10.4.5(a) shows the measured output noise PSD where the gain of amplifier is 1072, and thus the input-referred noise voltage of 13.5nV/√Hz is derived. For a low-frequency noise measurement below 10Hz, a time-domain filtered output peak-to-peak noise voltage is observed as 28mVpp, which corresponds to the input-referred noise voltage of 414nVpp [Fig.10.4.5(b)]. The performance and comparison with the state-of-the-art designs are summarized in Fig. 10.4.6. The IA can operate over a temperature range between –40 to 125°C and the offset drift is less than 25nV/°C. In addition, a drift of the ripple voltage in the above temperature range is measured as 3.3μV/°C. The stable gain limit is ±30dB and the worst-case GBW is 32MHz. This means that the GBW/\(\sup_{\text{sup}}\) factor of 165 is accomplished. The NEF of the proposed IA is calculated as 7.2. Based on the measurement results of 12 samples, it is confirmed that the proposed IA achieves a small area, low power and low noise compared to the state-of-the-art designs.

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References:
Figure 10.4.1: Block diagram of the current-feedback instrumentation amplifier with digital calibration for automatic differential-pair matching (ADPM).

Figure 10.4.2: Detailed block diagram of the detector and calibration logic.

Figure 10.4.3: Timing diagram of the calibration scheme.

Figure 10.4.4: Measured input-referred ripple voltage; (a) before and (b) after calibration.

Figure 10.4.5: Measured output noise; (a) PSD with the amplifier gain of 1072, and (b) 0.1-10Hz time-domain output waveform with the gain of 67608.

Figure 10.4.6: Performance summary and comparison.
Figure 10.4.7: Chip micrograph.